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DATA SHEET

BLF245 VHF power MOS transistor

Product specification

September 1992

VHF power MOS transistor

BLF245

FEATURES

- High power gain
- Low noise figure
- Easy power control
- Good thermal stability
- Withstands full load mismatch.

DESCRIPTION

Silicon N-channel enhancement mode vertical D-MOS transistor designed for large signal amplifier applications in the VHF frequency range.

The transistor is encapsulated in a 4-lead SOT123 flange envelope, with a ceramic cap. All leads are isolated from the flange.

Matched gate-source voltage (V_{GS}) groups are available on request.

PINNING - SOT123

| PIN | DESCRIPTION |
|-----|-------------|
| 1 | drain |
| 2 | source |
| 3 | gate |
| 4 | source |

PIN CONFIGURATION

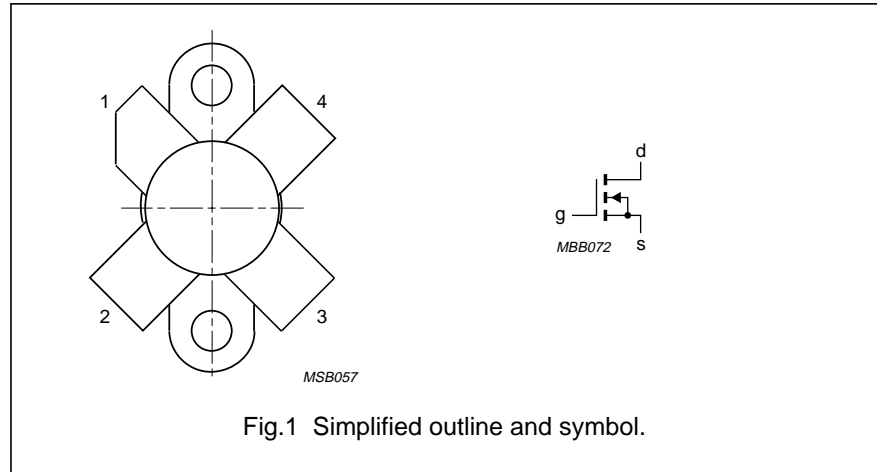


Fig.1 Simplified outline and symbol.

CAUTION

The device is supplied in an antistatic package. The gate-source input must be protected against static charge during transport and handling.

WARNING

Product and environmental safety - toxic materials
 This product contains beryllium oxide. The product is entirely safe provided that the BeO disc is not damaged. All persons who handle, use or dispose of this product should be aware of its nature and of the necessary safety precautions. After use, dispose of as chemical or special waste according to the regulations applying at the location of the user. It must never be thrown out with the general or domestic waste.

QUICK REFERENCE DATA

RF performance at $T_h = 25\text{ }^\circ\text{C}$ in a class-B test circuit.

| MODE OF OPERATION | f (MHz) | V_{DS} (V) | P_L (W) | G_p (dB) | η_D (%) |
|-------------------|---------|--------------|-----------|------------|--------------|
| CW, class-B | 175 | 28 | 30 | > 13 | > 50 |

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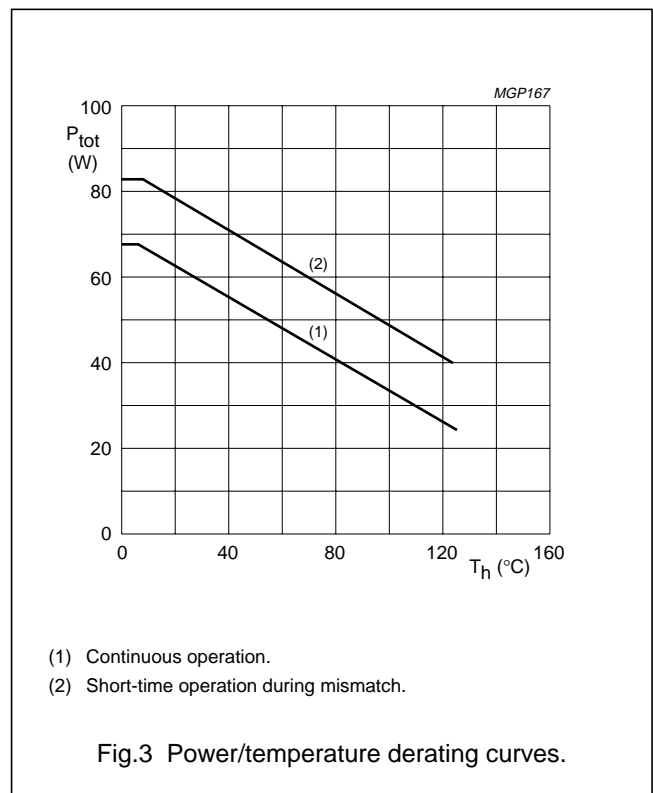
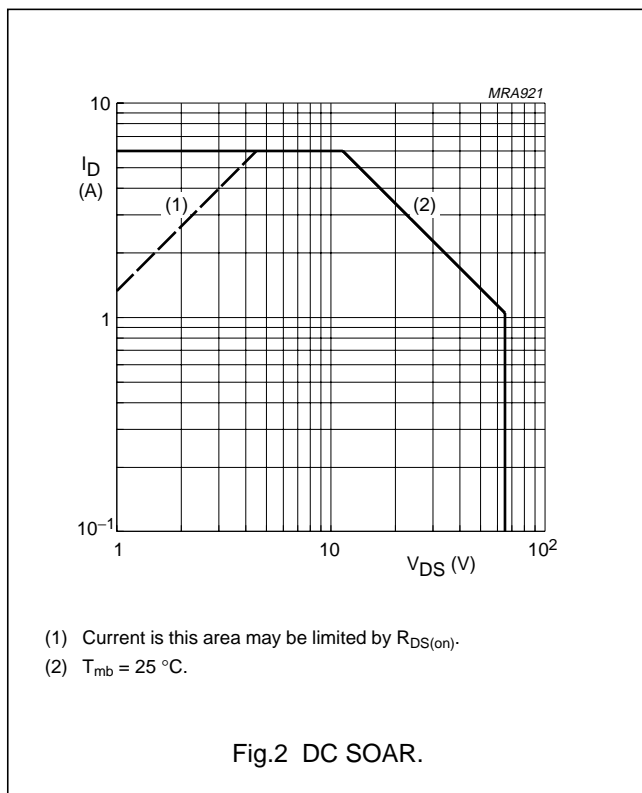
LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | UNIT |
|--------------|-------------------------|---|------|------|------------------|
| V_{DS} | drain-source voltage | $V_{GS} = 0$ | – | 65 | V |
| $\pm V_{GS}$ | gate-source voltage | $V_{DS} = 0$ | – | 20 | V |
| I_D | DC drain current | | – | 6 | A |
| P_{tot} | total power dissipation | up to $T_{mb} = 25\text{ }^\circ\text{C}$ | – | 68 | W |
| T_{stg} | storage temperature | | –65 | 150 | $^\circ\text{C}$ |
| T_j | junction temperature | | – | 200 | $^\circ\text{C}$ |

THERMAL RESISTANCE

| SYMBOL | PARAMETER | CONDITIONS | THERMAL RESISTANCE |
|----------------|---|--|--------------------|
| $R_{th\ j-mb}$ | thermal resistance from junction to mounting base | $T_{mb} = 25\text{ }^\circ\text{C}; P_{tot} = 68\text{ W}$ | 2.6 K/W |
| $R_{th\ mb-h}$ | thermal resistance from mounting base to heatsink | $T_{mb} = 25\text{ }^\circ\text{C}; P_{tot} = 68\text{ W}$ | 0.3 K/W |



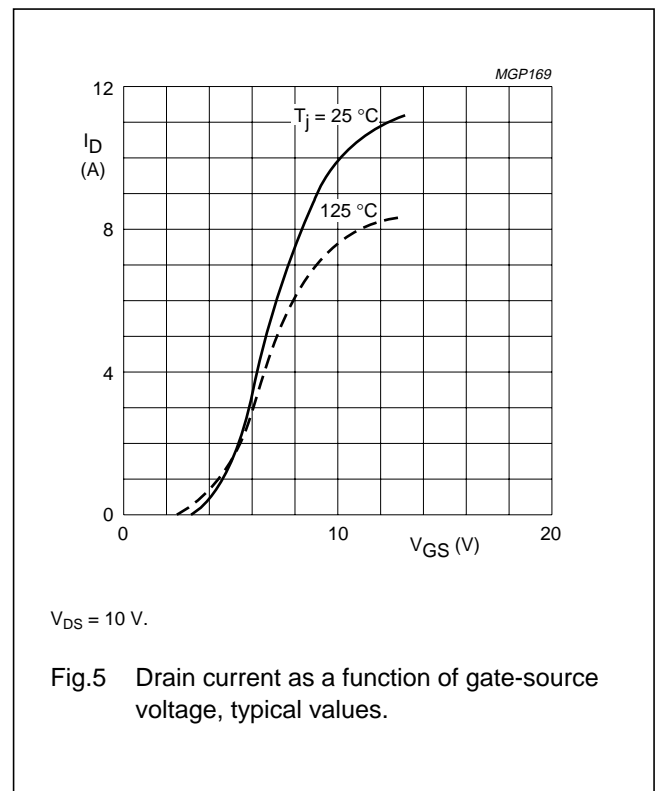
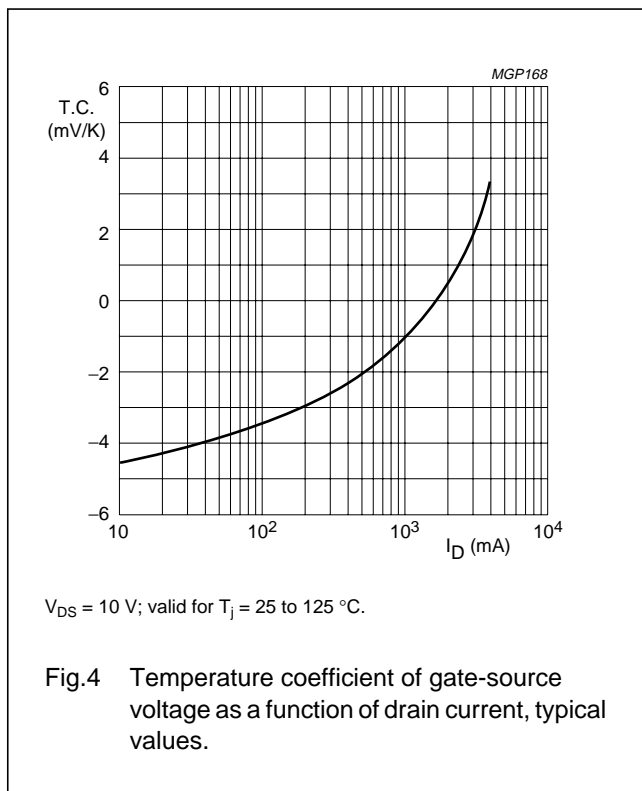
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CHARACTERISTICS

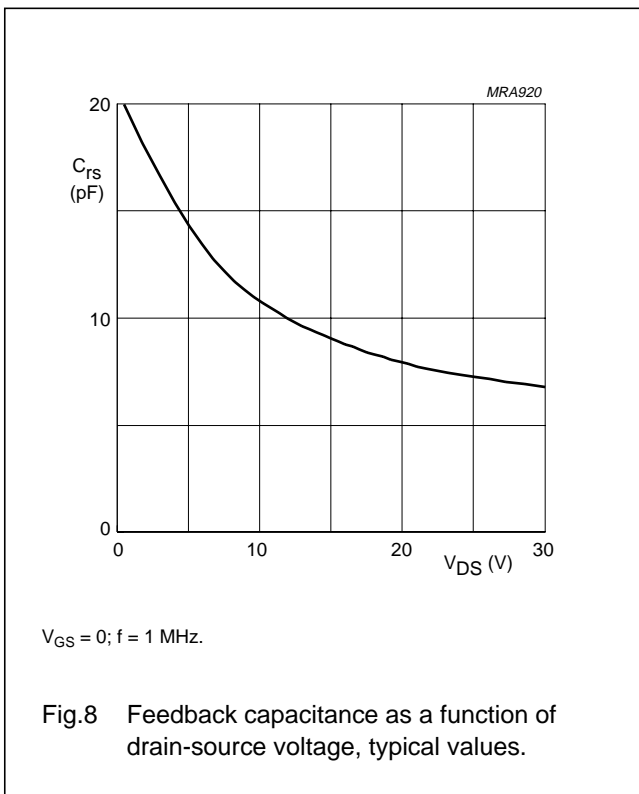
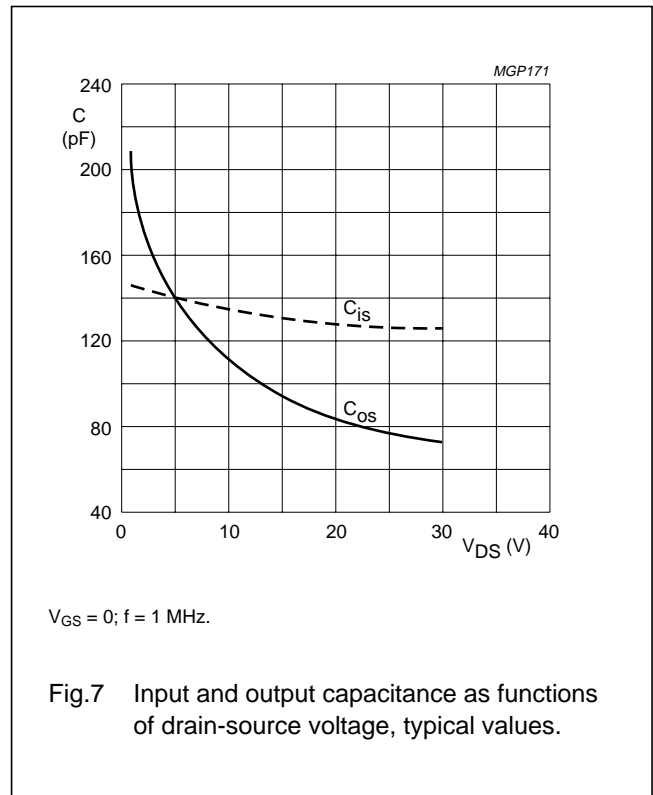
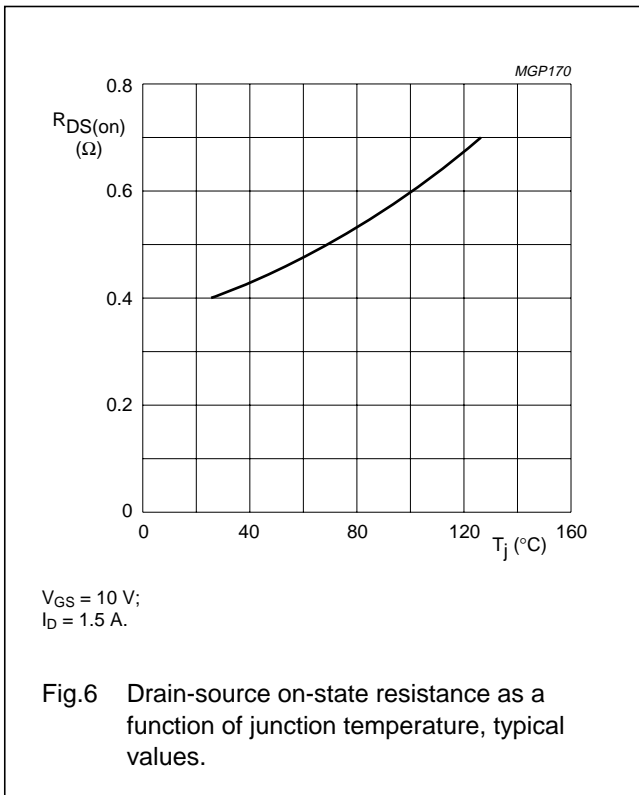
$T_j = 25\text{ }^\circ\text{C}$ unless otherwise specified.

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|-----------------|---|---|------|------|------|---------------|
| $V_{(BR)DSS}$ | drain-source breakdown voltage | $V_{GS} = 0; I_D = 10\text{ mA}$ | 65 | – | – | V |
| I_{DSS} | drain-source leakage current | $V_{GS} = 0; V_{DS} = 28\text{ V}$ | – | – | 2 | mA |
| I_{GSS} | gate-source leakage current | $\pm V_{GS} = 20\text{ V}; V_{DS} = 0$ | – | – | 1 | μA |
| $V_{GS(th)}$ | gate-source threshold voltage | $I_D = 10\text{ mA}; V_{DS} = 10\text{ V}$ | 2 | – | 4.5 | V |
| ΔV_{GS} | gate-source voltage difference of matched devices | $I_D = 10\text{ mA}; V_{DS} = 10\text{ V}$ | – | – | 100 | mV |
| g_{fs} | forward transconductance | $I_D = 1.5\text{ A}; V_{DS} = 10\text{ V}$ | 1.2 | 1.9 | – | S |
| $R_{DS(on)}$ | drain-source on-state resistance | $I_D = 1.5\text{ A}; V_{GS} = 10\text{ V}$ | – | 0.4 | 0.75 | Ω |
| I_{DSX} | on-state drain current | $V_{GS} = 10\text{ V}; V_{DS} = 10\text{ V}$ | – | 10 | – | A |
| C_{is} | input capacitance | $V_{GS} = 0; V_{DS} = 28\text{ V}; f = 1\text{ MHz}$ | – | 125 | – | pF |
| C_{os} | output capacitance | $V_{GS} = 0; V_{DS} = 28\text{ V}; f = 1\text{ MHz}$ | – | 75 | – | pF |
| C_{rs} | feedback capacitance | $V_{GS} = 0; V_{DS} = 28\text{ V}; f = 1\text{ MHz}$ | – | 7 | – | pF |
| F | noise figure (see Fig.14) | input and output power matched for: $I_D = 1\text{ A}; V_{DS} = 28\text{ V}; P_L = 30\text{ W};$ $R_1 = 1\text{ k}\Omega; T_h = 25\text{ }^\circ\text{C}; f = 175\text{ MHz}$ | – | 2 | – | dB |



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APPLICATION INFORMATION FOR CLASS-B OPERATION

$T_h = 25\text{ }^\circ\text{C}$; $R_{th\text{ mb-h}} = 0.3\text{ K/W}$; $R1 = 1\text{ k}\Omega$.

RF performance in CW operation in a common source class-B test circuit.

| MODE OF OPERATION | f (MHz) | V _{DS} (V) | I _{DQ} (mA) | P _L (W) | G _p (dB) | η_D (%) | Z _i (Ω) (note 1) | Z _L (Ω) |
|-------------------|---------|---------------------|----------------------|--------------------|---------------------|-----------------|--------------------------------------|-----------------------------|
| CW, class-B | 175 | 28 | 50 | 30 | > 13 typ. 15.5 | < 50 typ. 67 | 2.0 – j2.7 | 3.9 + j4.4 |
| | 175 | 12.5 | 50 | 12 | typ. 12 | typ. 66 | 2.4 – j2.5 | 3.8 + j1.3 |

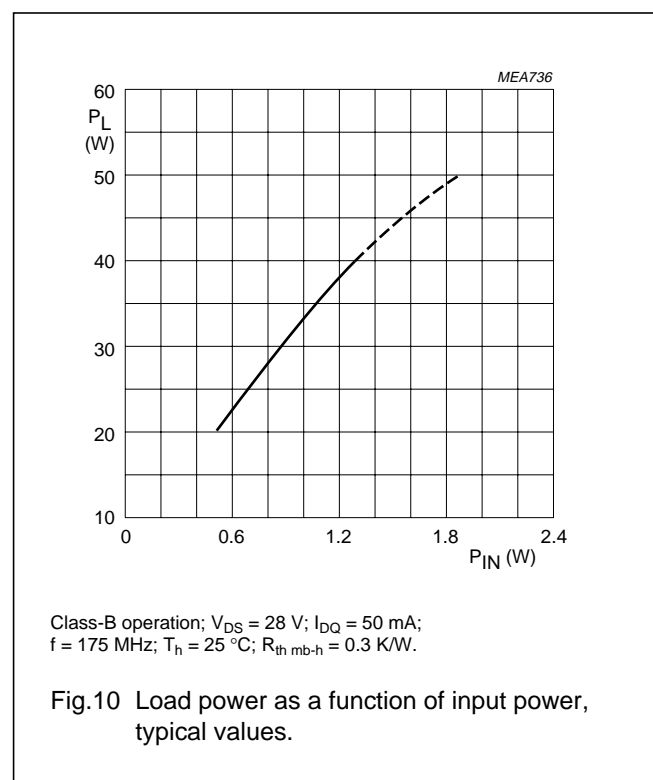
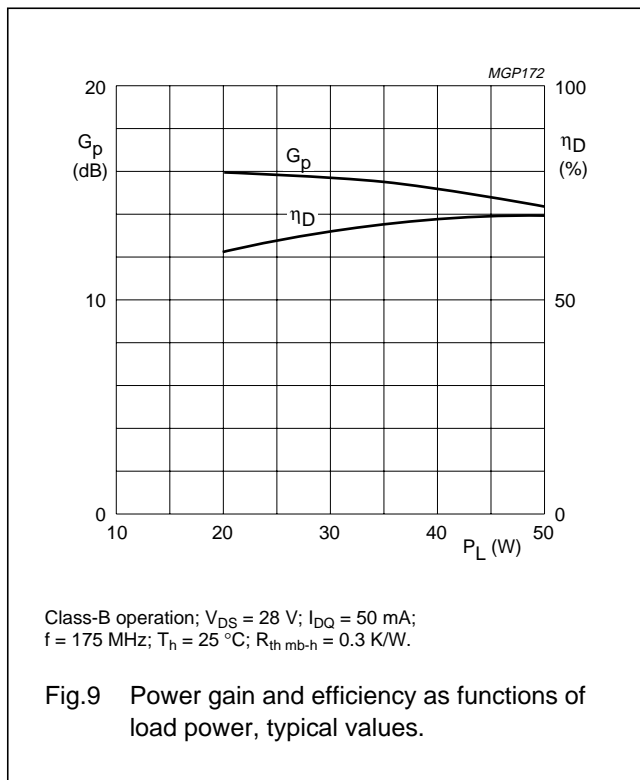
Note

1. R1 included.

Ruggedness in class-B operation

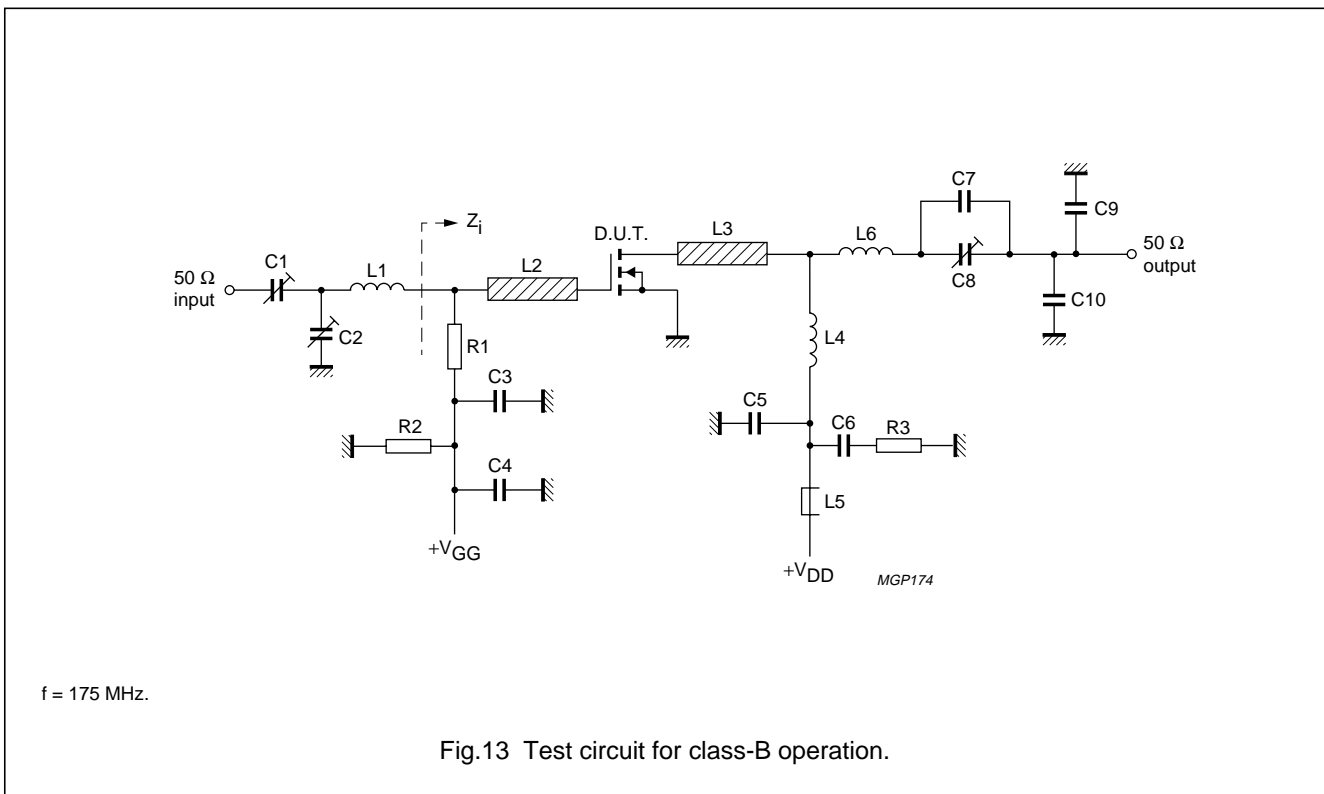
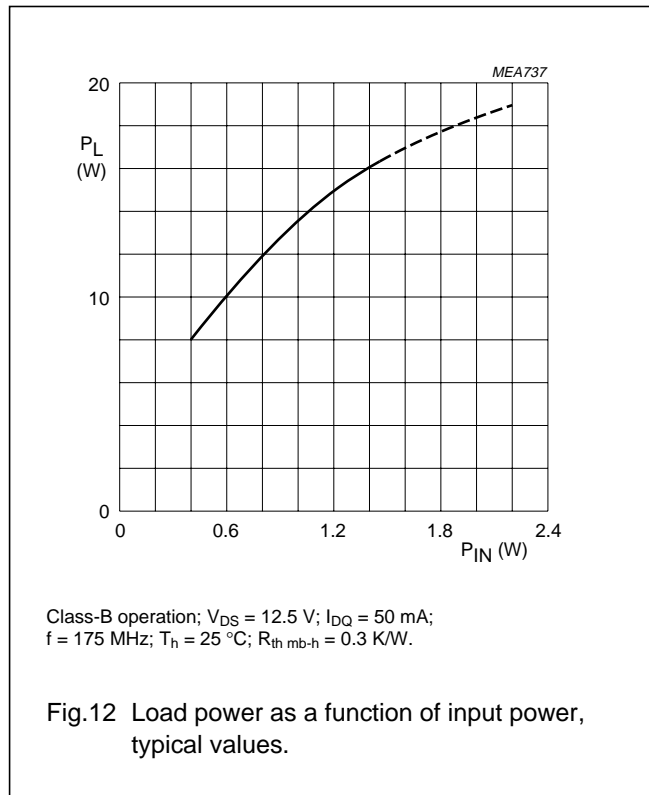
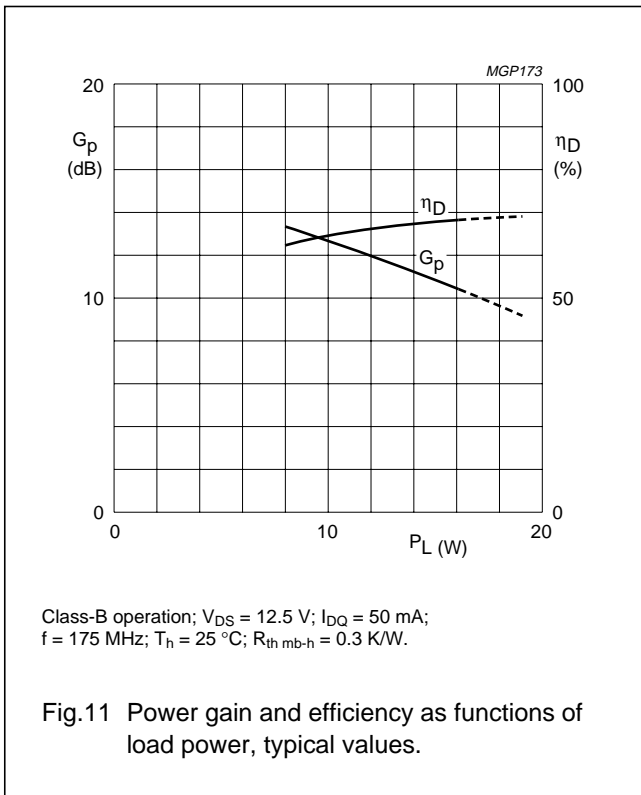
The BLF245 is capable of withstanding a load mismatch corresponding to VSWR = 50 through all phases under the following conditions:

$T_h = 25\text{ }^\circ\text{C}$; $R_{th\text{ mb-h}} = 0.3\text{ K/W}$; at rated load power.



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List of components (class-B test circuit)

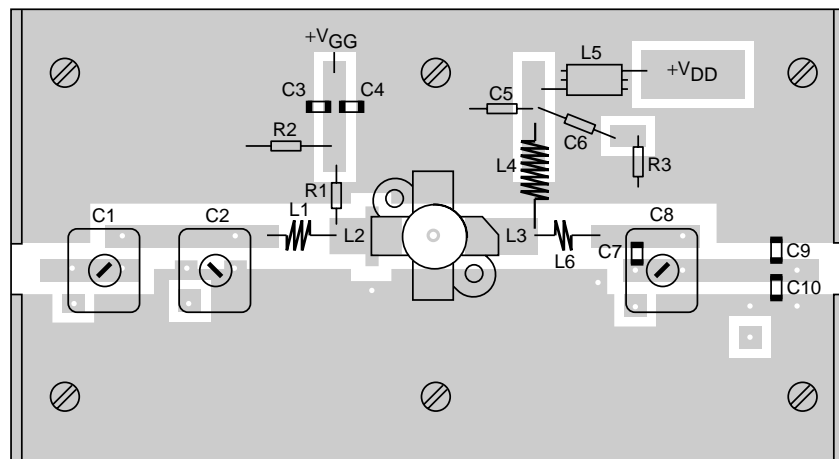
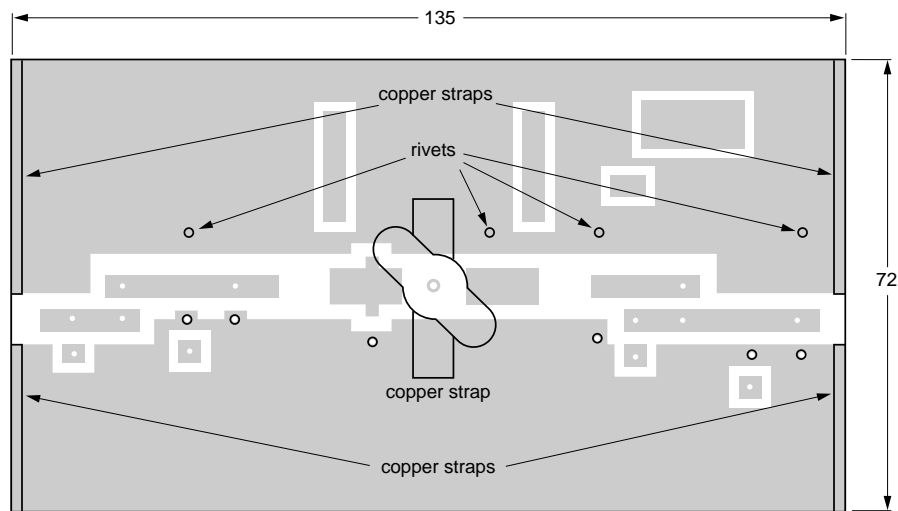
| COMPONENT | DESCRIPTION | VALUE | DIMENSIONS | CATALOGUE NO. |
|-----------|---|------------|--|----------------|
| C1 | film dielectric trimmer | 4 to 40 pF | | 2222 809 07008 |
| C2, C8 | film dielectric trimmer | 5 to 60 pF | | 2222 809 07011 |
| C3 | multilayer ceramic chip capacitor | 100 pF | | 2222 854 13101 |
| C4, C6 | multilayer ceramic chip capacitor | 100 nF | | 2222 852 47104 |
| C5 | ceramic capacitor | 100 pF | | 2222 680 10101 |
| C7 | multilayer ceramic chip capacitor (note 1) | 18 pF | | |
| C9 | multilayer ceramic chip capacitor (note 1) | 27 pF | | |
| C10 | multilayer ceramic chip capacitor (note 1) | 24 pF | | |
| L1 | 3 turns enamelled 0.5 mm copper wire | 13.5 nH | length 3.5 mm int. dia. 2 mm leads 2 × 2 mm | |
| L2, L3 | stripline (note 2) | 30 Ω | 10 × 6 mm | |
| L4 | 6 turns enamelled 1.5 mm copper wire | 98 nH | length 12.5 mm int. dia. 5 mm leads 2 × 2 mm | |
| L5 | grade 3B Ferroxcube RF choke | | | 4312 020 36640 |
| L6 | 2 turns enamelled 1.5 mm copper wire | 24.5 nH | length 4 mm int. dia. 5 mm leads 2 × 2 mm | |
| R1 | metal film resistor | 1 kΩ | | |
| R2 | metal film resistor | 1 MΩ | | |
| R3 | metal film resistor | 10 Ω | | |

Notes

1. American Technical Ceramics (ATC) capacitor, type 100B or other capacitor of the same quality.
2. The striplines are mounted on a double copper-clad PCB with epoxy fibre-glass dielectric ($\epsilon_r = 4.5$), thickness $\frac{1}{16}$ inch.

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MGP175

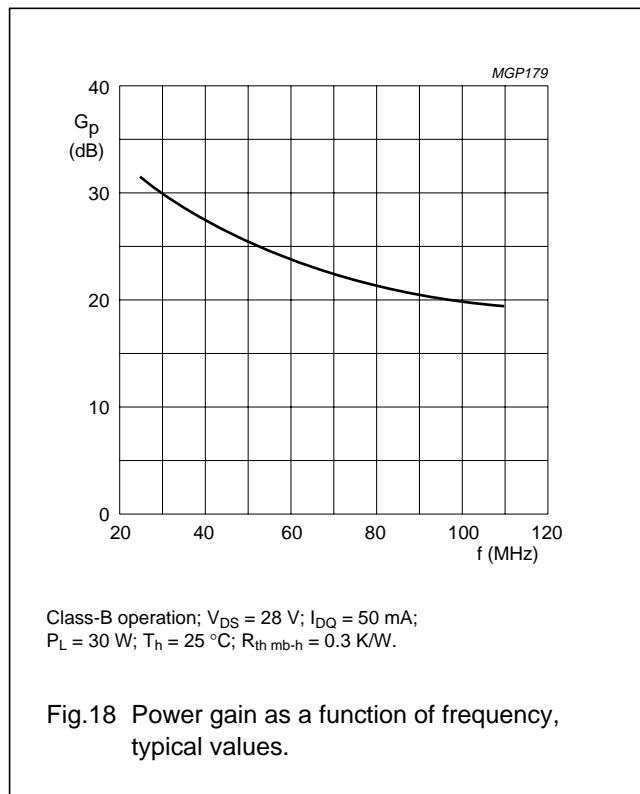
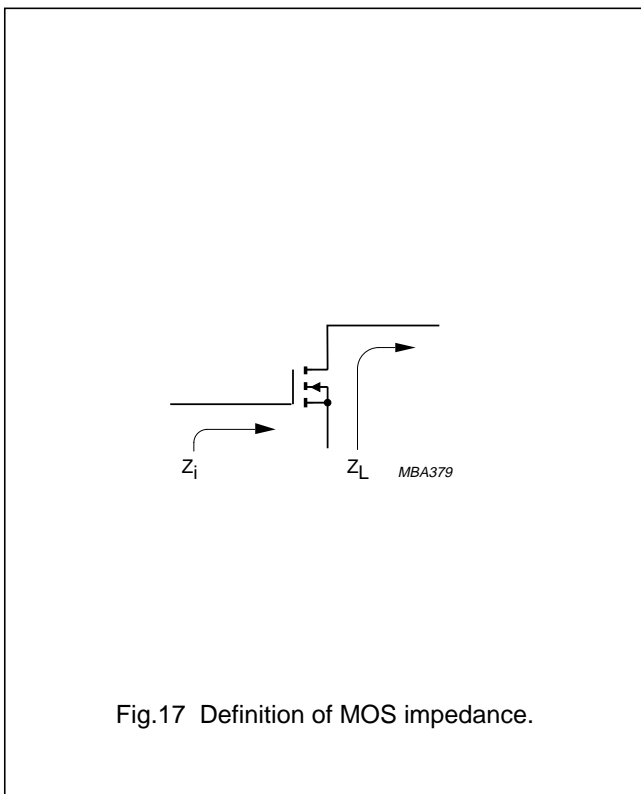
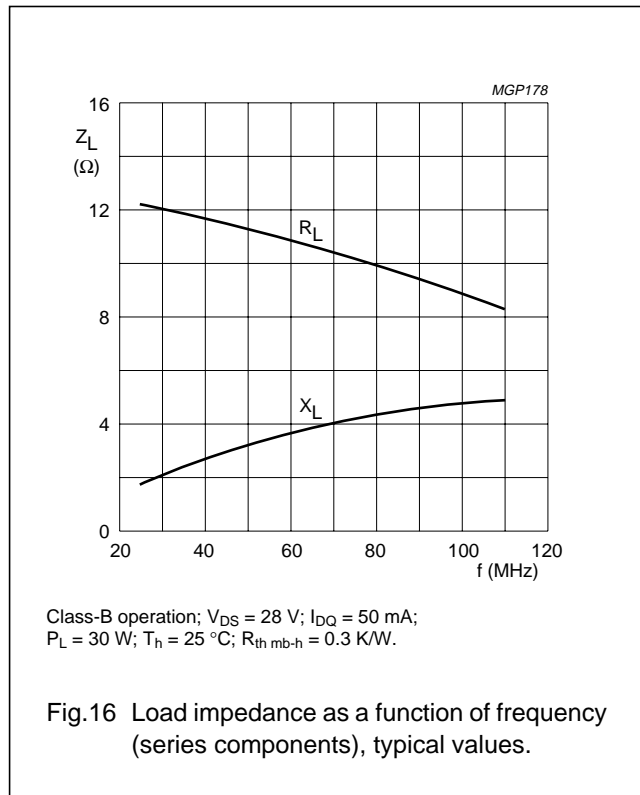
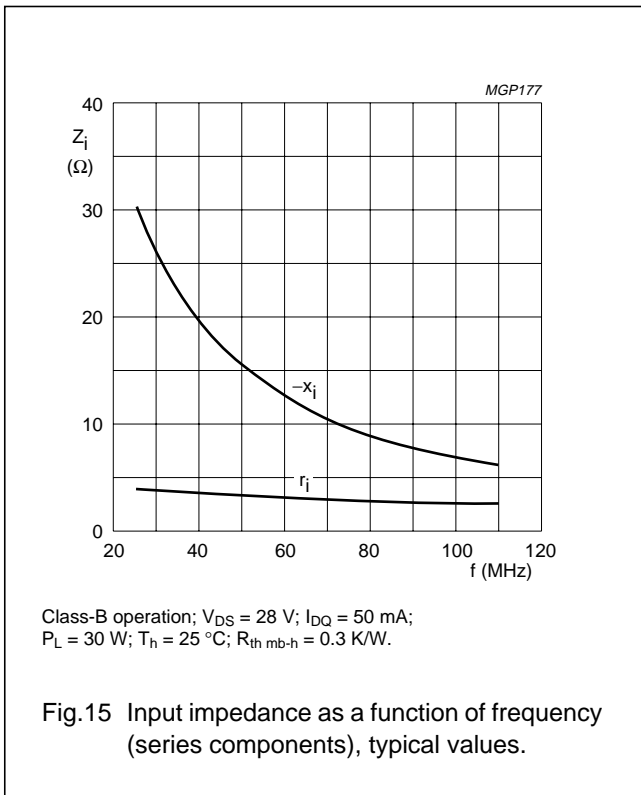
The circuit and components are situated on one side of the epoxy fiber-glass board; the other side is unetched copper and serves as an earth. Earth connections are made by means of fixing screws, hollow rivets and copper straps under the sources and around the edges, to provide a direct contact between the copper on the component side and the ground plane.

Dimensions in mm.

Fig.14 Component layout for 175 MHz class-B test circuit.

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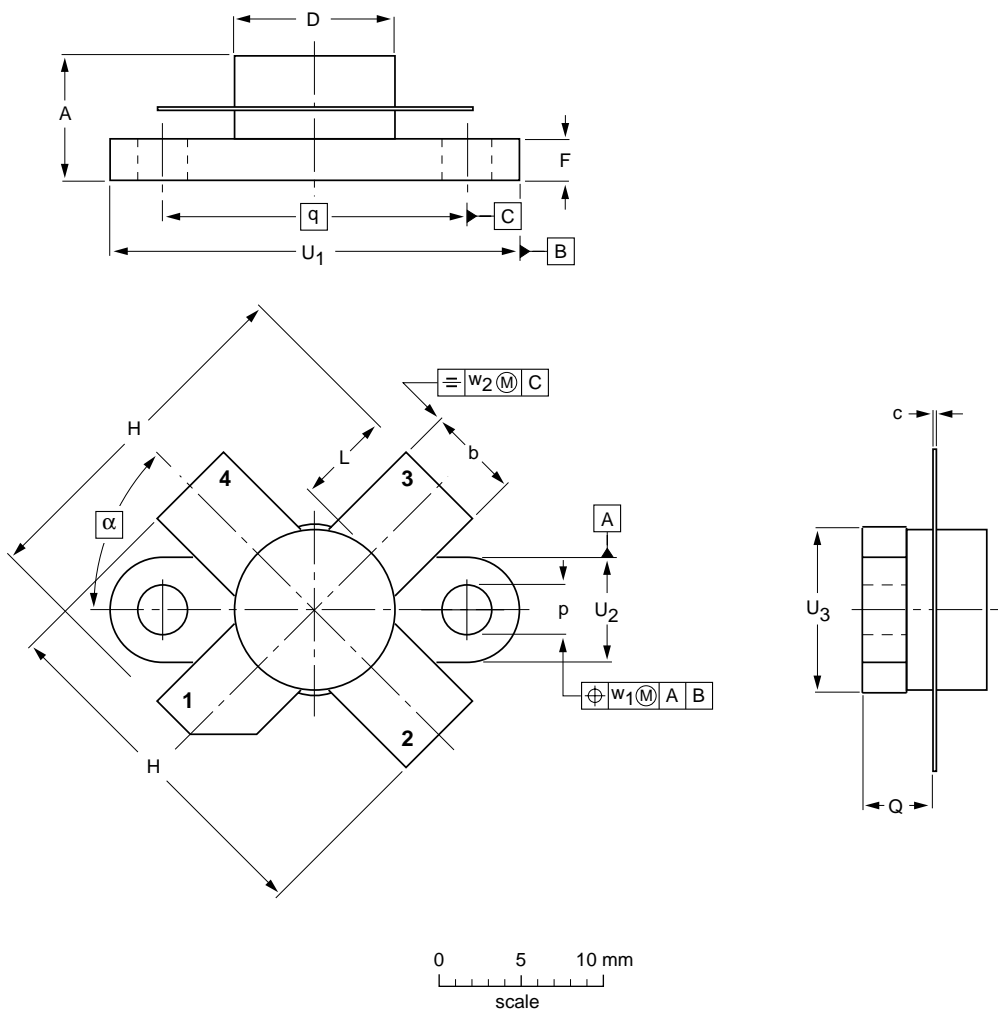
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PACKAGE OUTLINE

Flanged ceramic package; 2 mounting holes; 4 leads

SOT123A



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

| UNIT | A | b | c | D | D ₁ | F | H | L | p | Q | q | U ₁ | U ₂ | U ₃ | w ₁ | w ₂ | α |
|--------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|-------|----------------|----------------|----------------|----------------|----------------|-----|
| mm | 7.47 6.37 | 5.82 5.56 | 0.18 0.10 | 9.73 9.47 | 9.63 9.42 | 2.72 2.31 | 20.71 19.93 | 5.61 5.16 | 3.33 3.04 | 4.63 4.11 | 18.42 | 25.15 24.38 | 6.61 6.09 | 9.78 9.39 | 0.51 | 1.02 | 45° |
| inches | 0.294 0.251 | 0.229 0.219 | 0.007 0.004 | 0.383 0.373 | 0.397 0.371 | 0.107 0.091 | 0.815 0.785 | 0.221 0.203 | 0.131 0.120 | 0.182 0.162 | 0.725 | 0.99 0.96 | 0.26 0.24 | 0.385 0.370 | 0.02 | 0.04 | |

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|-----------------|------------|-------|------|--|---------------------|------------|
| | IEC | JEDEC | EIAJ | | | |
| SOT123A | | | | | | 97-06-28 |

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DEFINITIONS

| Data Sheet Status | |
|---|---|
| Objective specification | This data sheet contains target or goal specifications for product development. |
| Preliminary specification | This data sheet contains preliminary data; supplementary data may be published later. |
| Product specification | This data sheet contains final product specifications. |
| Limiting values | |
| Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability. | |
| Application information | |
| Where application information is given, it is advisory and does not form part of the specification. | |

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